A METHOD FOR FORMING A THIN COMPLETE HIGH-PERMITTIVITY DIELECTRIC LAYER

DESCRIPTION

FIELD OF THE INVENTION

[Para 1] The present invention is related to semiconductor processing, and more particularly, to a method for forming a thin complete high-permittivity dielectric layer for semiconductor applications.

BACKGROUND OF THE INVENTION

[Para 2] In the semiconductor industry, the minimum feature sizes of microelectronic devices are approaching the deep sub-micron regime to meet the demand for faster, lower power microprocessors and digital circuits. Downscaling of complementary metal-oxide semiconductor (CMOS) devices imposes scaling constraints on the dielectric material in gate stacks, where the thickness of the standard SiO_2 gate oxide dielectric layer is approaching the limit (~10 Angstroms (Å)) at which tunneling currents significantly impact transistor performance.

[Para 3] To increase device reliability and reduce electron leakage from the gate electrode to the transistor channel, semiconductor transistor technology is using high-permittivity dielectric materials (also referred to herein as "high-k" materials) in gate stacks that allow increased physical thickness of the gate dielectric layer while maintaining an equivalent gate oxide thickness (EOT) of less than about 15 Å. EOT is a relative measure of the thickness of a gate dielectric material with respect to the actual physical thickness of a SiO_2 layer having the same capacitance value as the gate dielectric material. Since capacitance is directly proportional to the dielectric constant and inversely proportional the thickness of the layer, it follows that an increase in dielectric constant allows for an increase in thickness in order to maintain the same capacitance.

[Para 4] Dielectric materials featuring a dielectric constant greater than that of SiO_2 (k~3.9) are commonly referred to as high-k materials. In addition, high-k materials may refer to dielectric materials that are deposited onto the substrate (e.g., HfO_2, ZrO_2) rather than dielectric materials that are grown on the surface of the substrate (e.g., SiO_2, SiO_xN_y). High-k materials may incorporate metallic silicates or oxides, including Ta_2O_5 (k~26), TiO_2 (k~80), ZrO_2 (k~25), Al_2O_3 (k~9), $HfSiO_x$ (k~4-25), and

HfO_2 (k~25). Manufacturing of features having sizes in the sub-micron regime can require formation of very thin high-k layers (i.e., having thickness less than about 100 Å) with a minimum of gaps or variations in the thickness of the high-k layer.

SUMMARY OF THE INVENTION

[Para 5] A method is provided for forming a thin complete high-k layer on a substrate. The method provides a process for forming a thin complete high-k layer with a minimum of gaps and with good thickness uniformity. The method includes providing a substrate in a process chamber, depositing a thick complete high-k layer on the substrate, and thinning the deposited high-k layer to form a thin complete high-k layer on the substrate. The thinning can include a reactive plasma etch process to remove a portion of the deposited high-k layer or, alternately, a plasma process to modify/thin the deposited high-k layer and remove the modified portion of the high-k layer using wet processing.

[Para 6] In one embodiment of the invention, the thick complete high-k layer can have a thickness between about 30 Å and about 200 Å. Alternately, the thickness of the thick complete high-k layer can be between about 50 Å and about 100 Å. It may be appreciated that the minimum thickness necessary to form a complete layer may differ from one high-k material to another. The minimum thickness, however, is typically greater than the desired thickness for that high-k material in the gate stack. Thus, after the complete high-k layer is achieved, a portion of that layer is removed, i.e., thinned, to leave a complete high-k layer of the thinner desired thickness. In one embodiment of the invention, the thin complete high-k layer can have a thickness between about 5 Å and about 50 Å. Alternately, the thickness of the thin complete high-k layer can between about 30 Å and about 40 Å.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 7] In the accompanied drawings:

[Para 8] FIGS. 1A-1B show schematic cross-sectional representations of gate stacks containing a high-k layer made according to embodiments of the present invention;

[Para 9] FIGS. 2A-2D schematically show formation of a thin complete high-k layer on a substrate according to an embodiment of the present invention;

[Para 10] FIGS. 2E-2F schematically show formation of a thin complete high-k layer on a substrate according to another embodiment of the present invention;

[Para 11] FIG. 3 is a flowchart illustrating a method of forming a thin complete high-k layer according to an embodiment of the invention;

[Para 12] FIG. 4 schematically shows a processing system configured for depositing a high-k layer according to an embodiment of the invention;

[Para 13] FIG. 5 schematically shows a plasma processing system configured for processing a high-k layer according to an embodiment of the present invention;

[Para 14] FIG. 6 schematically shows a plasma processing system configured for processing a high-k layer according to another embodiment of the present invention;

[Para 15] FIG. 7 schematically shows a plasma processing system configured for processing a high-k layer according to yet another embodiment of the present invention; and

[Para 16] FIG. 8 schematically shows a plasma processing system configured for processing a high-k layer according to still another embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[Para 17] FIGS. 1A-1B show schematic cross-sectional representations of gate stacks containing a high-k layer made according to embodiments of the present invention. FIG. 1A shows a partially completed gate stack 100 after an anisotropic plasma etch process that forms the etch features shown. The exemplary gate stack 100 contains a substrate 102 having a source region 113 and a drain region 114, a dielectric interface layer 104, a high-k layer 106, a gate electrode layer 108, an anti-reflective coating (ARC)/hardmask layer 110, and a photoresist layer 112. The substrate 102 can, for example, contain Si, Ge, Si/Ge, or GaAs. In one embodiment of the invention, the substrate 102 can be a Si substrate containing epitaxial Si or poly-Si. A Si substrate can be of n- or p-type, depending on the type of device being formed. The substrate 102 can be of any size, for example a 200 mm substrate, a 300 mm substrate, or an even larger substrate.

[Para 18] The dielectric interface layer 104 can, for example, be an oxide layer (e.g., SiO_2), a nitride layer (e.g., SiN_x), or an oxynitride layer (e.g., SiO_xN_y), or a combination thereof. The dielectric interface layer 104 at the substrate surface can preserve interface state characteristics and form an interface with good electrical properties between the high-k layer 106 and the substrate 102. However, the presence of an interface layer 104 lowers the overall dielectric constant of the gate stack 100 and, therefore, when integrated with the thin high-k layer 106, the interface layer 104 may need to be very thin. Integrated circuits containing a Si substrate commonly employ SiO_2 and/or SiO_xN_y interface layers that can have excellent electrical properties, including high electron mobility and low electron trap densities. Currently, gate stacks containing a high-k layer formed on SiO_2 and/or SiO_xN_y interface layers can require an interface layer thickness of only about 5-10 Å.

[Para 19] The high-k layer is formed in accordance with the method of the present invention, as described in further detail below. The high-k layer 106 can, for example, contain a metal oxide or a metal silicate, including Ta_2O_5, TiO_2, ZrO_2, Al_2O_3, Y_2O_3, $HfSiO_x$, HfO_2, $ZrSiO_x$, $TaSiO_x$, SrO_x, $SrSiO_x$, LaO_x, $LaSiO_x$, YO_x, or $YSiO_x$, or combinations of two or more thereof. The thickness of the high-k layer 106 can, for example, be between about 5 Å and about 50 Å, and can be about 30-40 Å. The gate electrode layer 108 in FIG. 1A can, for example, be doped poly-Si. Selection of the appropriate ARC/hardmask layer 110 and photoresist layer 112 that enables formation of etch features with the desired dimensions are well known to persons skilled in the art of lithography and plasma etching.

[Para 20] FIG. 1B shows another partially completed gate stack 101 after an anisotropic plasma etch process that forms the etch features shown. The gate stack 101 contains a metal gate electrode layer 107 in addition to the materials layers shown in FIG. 1A. The metal gate electrode layer 107 can, for example, be about 100 Å thick and can contain W, WN, Al, TaN, TaSiN, HfN, HfSiN, TiN, TiSiN, Re, Ru, or SiGe. The introduction of metal gate electrodes to replace or to be integrated with the traditional poly-Si gate electrode layer can bring about several advantages, including elimination of the poly-silicon gate depletion effect, reduction in sheet resistance, better reliability and potentially better thermal stability on advanced high-k layers.

[Para 21] FIGS. 2A-2D schematically show formation of a thin complete high-k layer on a substrate according to an embodiment of the present invention. FIG. 2A shows a substrate structure 200 including a substrate 202 having a dielectric interface layer 204 formed thereon. As described above, the interface layer 204 can, for example, be an oxide layer, a nitride layer, or an oxynitride layer, or a combination thereof. Processes

for forming oxide, nitride, and oxynitride layers are well known to those skilled in the of semiconductor processing. Alternately, the interface layer 204 may not be present.

[Para 22] In general, different modes of film growth can be encountered when depositing a thin film on substrate. A Frank-Van der Merwe thin film growth is characterized by an ideal epitaxial layer by layer growth on a substrate, whereas a Volmer-Weber thin film growth is characterized by island growth on a substrate. A Stranski-Krastanov thin film growth is characterized by island growth coupled with a layer by layer growth on a substrate. With high-k materials, the Volmer-Weber and/or Stranski-Krastanov growth mode is/are frequently observed.

[Para 23] FIG. 2B shows islands of high-k material 203 formed on the interface layer 204. As described above, the high-k material 203 can contain a metal oxide or a metal silicate, or a combination thereof. FIG. 2B illustrates Volmer-Weber growth when depositing a high-k material 203 on an interface layer 204. Instead of forming a thin complete high-k layer with no gaps and good thickness uniformity (Frank-Van der Merwe growth mode), the deposition process depicted in FIG. 2B forms islands of the deposited high-k material 203 with gaps that expose the interface layer 204 between the high-k islands. In FIG. 2B, the islands have a thickness D_{203} that can, for example, be between about 5 Å and about 50 Å, or greater. The thickness D_{203} and the lateral size of the islands can vary depending on the type of the high-k material 203 and the type of the interface layer 204. Furthermore, the thickness D_{203} and the lateral size of the islands can depend on the deposition and annealing conditions of the high-k material 203 and the interface layer 204.

[Para 24] The high-k material 203 can, for example, be deposited onto the interface layer 204 using various deposition processes that are well-known to persons skilled in the art of thin film deposition, including, but not limited to, thermal chemical vapor deposition (TCVD), plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), and physical vapor deposition (PVD). An exemplary processing system configured for depositing a high-k layer on a substrate in a TCVD process is shown and described in FIG. 4.

[Para 25] One requirement for integrating a high-k material into the substrate structure 200 is that the high-k material 203 form a complete layer on the interface layer 204 (or on the substrate 202 when an interface layer is not present) and that the complete layer have good thickness uniformity. A complete high-k layer with good thickness uniformity is required to increase device reliability and reduce electron leakage from a gate electrode overlying the high-k material 203 to the substrate 202.

[Para 26] Further deposition of the high-k material onto the substrate structure 200 in FIG. 2B, results in a thick complete high-k layer 206 on the interface layer 204, as shown in FIG. 2C. A complete high-k layer is referred to herein as a high-k layer that completely covers, e.g., is continuous over, the underlying interface layer 204 or the substrate 202 without any gaps. The thick complete high-k layer 206 can, for example, have a thickness D_{206} between about 30 Å and about 200 Å with good thickness uniformity. As noted above, the minimum thickness to which the high-k layer must be deposited before a complete layer is achieved may vary among high-k materials, but generally is greater than 50 Å. However, the thickness D_{206} can be too great for many semiconductor devices that can, for example, require a thickness D_{206} that is between about 10 Å and about 40 Å. A thin complete high-k layer with a thickness less than D_{206} cannot simply be deposited onto the interface layer 204. Thus, by the method of the present invention, the complete high-k layer of thickness D_{206} is first formed, then thinned to achieve the desired thickness less than D_{206}.

[Para 27] FIG. 2D shows formation of a thin complete high-k layer 207 according to an embodiment of the invention. The thin complete high-k layer 207 is formed by first depositing the thick complete high-k layer 206 shown in FIG. 2C, and then thinning the layer 206 to form a thin complete high-k layer 207 with a thickness D_{207}, where the thickness D_{207} is less than D_{206}. According to one embodiment of the invention, the thickness D_{206} can be between about 30 Å and about 200 Å. Alternately, the thickness D_{206} can be between about 50 Å and about 100 Å. According to one embodiment of the invention, the thickness D_{207} can be between about 5 Å and about 50 Å. Alternately, the thickness D_{207} can be between about 30 Å and about 40 Å.

[Para 28] According to an embodiment of the invention, thinning of the thick complete high-k layer 206 can be performed in a plasma processing system. According to an embodiment of the present invention, the thinning can be carried out by reactive plasma etching of the high-k layer 206 using aggressive halogen-containing gases that react with the high-k layer 206 to form halogen-containing etch products that are removed from the plasma processing system. Halogen-containing gases with general formulas HX, X_2, C_xX_z, or $C_xH_yX_z$, where X is a halogen, can be used.

[Para 29] FIGS. 2E-2F schematically show formation of a thin complete high-k layer on a substrate according to another embodiment of the present invention. Thinning of the thick complete high-k layer 206 in FIG. 2C can be performed by a plasma modifying/thinning process that is combined with wet processing. Ion bombardment can be used to partially remove and/or modify the high-k layer 206 in FIG. 2F without completely removing it.

[Para 30] FIG. 2E schematically shows a modified portion 206a following a plasma modifying/thinning process performed on the high-k layer 206. In one example, the plasma can contain a reactive gas, for example HBr or HCl, and an inert gas. In another example, the plasma may only contain chemically inert gas species that are non-reactive towards the high-k layer 206 in a plasma environment, but where the ions have sufficient energy to effectively disrupt and/or thin the high-k layer 206 so that a subsequent wet etching process is able to efficiently remove the disrupted (modified) portion 206a from the un-modified portion 206b. The inert gas can, for example, contain the noble gases He, Ne, Ar, Kr, and Xe. The exact effect of the plasma modifying/thinning process can depend on the gases used in the plasma processing. It is believed that the plasma processing may increase the amorphous content of the high-k layer 206 and possibly break chemical bonds that create atomic fragments in the portion 206a. The suggested disruption of the molecular structure of the portion 206a during plasma processing can allow for a greater choice of wet etch chemistries that have high etch selectivity for the modified portion 206a compared to the un-modified portion 206b, the interface layer 204, and the substrate 202. The subsequent wet etch process can, for example, utilize hot sulfuric acid (H_2SO_4) or hydrofluoric acid ($HF_{(aq)}$) to remove the modified portion 206a from the un-modified portion 206b, thereby forming a thin complete high-k layer 207 with a thickness D_{207}. Since the high-k layer 206b is not traversed during the plasma modifying/thinning process, the likelihood of damage occurring to the underlying interface layer 204 and substrate 202 is reduced. Wet processing for removing thin layers from substrates is well known to artisans skilled in the art of semiconductor processing.

[Para 31] Plasma processing of the high-k layer 206 can lead to an increase in the thickness of the interface layer 204. A method for minimizing the increase in the thickness of the interface layer 204 during plasma processing of the high-k layer 206 is described in U.S. Patent Application No. _____, filed on even date herewith and titled "A METHOD AND SYSTEM FOR FORMING A FEATURE IN A HIGH-K LAYER, the content of which is hereby incorporated by reference in its entirety.

[Para 32] FIG. 3 is a flowchart illustrating a method of forming a thin complete high-k layer according to an embodiment of the invention. The process 300 includes at 302, providing a substrate in a process chamber configured for depositing a high-k layer on the substrate. In one embodiment of the invention, the substrate can further contain an interface layer formed on the substrate. At 304, a high-k layer is deposited on the substrate. The deposition process is carried out for a desired amount of time to form a thick complete high-k layer on the substrate. At 306, the thick complete high-k layer is thinned to form a thin complete high-k layer. In one embodiment of the invention,

the thinning can be performed using reactive plasma etching. In another embodiment of the invention, the plasma processing can include a plasma modifying/thinning process followed by wet processing for removing the modified portion of the high-k layer from the unmodified portion of the high-k layer. As would be appreciated by those skilled in the art, each of the steps or stages in the flowchart of FIG. 3 may encompass one or more separate steps and/or operations. Accordingly, the recitation of only three steps in 302, 304, 306 should not be understood to limit the method of the present invention solely to three steps or stages. Moreover, each representative step or stage 302, 304, 306 should not be understood to be limited to only a single process.

[Para 33] FIG. 4 schematically shows a plasma processing system configured for depositing a high-k layer on a substrate according to an embodiment of the invention. In particular, the processing system 400 is configured for depositing a high-k layer on a substrate 406 in a TCVD process. The processing system 400 comprises a process chamber 402, a gas injection system 408, a pumping system 412, a process monitoring system 438, and a controller 436. The process chamber 402 comprises a substrate holder 404, upon which a substrate 406 to be processed is affixed. Substrate 406 can be transferred into and out of process chamber 402 through a slot valve (not shown) and chamber feed-through (not shown) via robotic substrate transfer system where it is received by substrate lift pins (not shown) housed within substrate holder 404 and mechanically translated by devices housed therein. Once the substrate 406 is received from the substrate transfer system, it is lowered to an upper surface of the substrate holder 404. The substrate 406 can, for example, be a Si substrate and, depending on the type of device being formed, can, for example, consist of a substrate of any diameter, for example, a 200 mm substrate, a 300 mm substrate, or an even larger substrate.

[Para 34] The substrate 406 can be affixed to the substrate holder 404 via an electrostatic clamp (not shown). Furthermore, the substrate holder 404 further includes a cooling system (not shown) including a re-circulating coolant flow that receives heat from the substrate holder 404 and transfers heat to a heat exchanger system (not shown), or when heating, transfers heat from the heat exchanger system. Moreover, gas may be delivered to the backside of the substrate 406 to improve the gas-gap thermal conductance between the substrate 406 and the substrate holder 404. Such a system is utilized when temperature control of the substrate 406 is required at elevated or reduced temperatures.

[Para 35] A gas injection system 408 introduces process gas 410 to the process chamber 402. The gas injection system 408 comprises a liquid delivery system (LDS)

420 that includes at least one precursor source 422 containing a high-k precursor material. The introduction of precursor material into vaporizer 426 can be controlled using a liquid mass flow controller (LMFC) 424. Vaporized precursor material from vaporizer 426 can be mixed with a carrier gas delivered via gas line 430 from gas box 428 and the mixture can be delivered to the process chamber 402 via gas line 434. Purge gases (e.g., Ar) and other gases (e.g., O_2, N_2, and H_2O) can be delivered directly from the gas box 428 to the process chamber 402 utilizing additional gas line 432. The gas injection system 408 allows independent control over the delivery of process gas 410 to the process chamber 402 from ex-situ gas sources. The gas injection system 408 can employ an effusive gas distribution source such as a showerhead in the process chamber 402. In an alternate embodiment of the invention, the gas injection system 408 can be configured for vaporizing a solid precursor material and delivering the vaporized precursor material via gas line 434 to the process chamber 402.

[Para 36] A vacuum pumping system 412 comprises a vacuum pump 418, a trap 416, and automatic pressure controller (APC) 414. The vacuum pump 418 can include a turbo-molecular vacuum pump (TMP) capable of a pumping speed up to 5000 liters per second (and greater) and a gate valve for throttling the chamber pressure. Alternatively, the vacuum pump 418 can include a dry pump. During processing, process gas 410 can be introduced into the process chamber 402 via the gas injection system 408 and the process pressure is adjusted by the APC 414. The trap 416 can collect un-reacted precursor material and by-products from the process chamber 402.

[Para 37] A controller 436 includes a microprocessor, a memory, and a digital I/O port capable of generating control voltages sufficient to communicate and activate inputs of the processing system 400 as well as monitor outputs from the processing system 400. Moreover, the controller 436 is coupled to and exchanges information with the process chamber 402, the process monitoring system 438, the gas injection system 408, and the vacuum pumping system 412. A program stored in the memory is utilized to control the aforementioned components of a processing system 400 according to a stored process recipe. One example of controller 436 is a DELL PRECISION WORKSTATION 610™, available from Dell Corporation, Dallas, Texas.

[Para 38] The process monitoring system 438 can, for example, measure gaseous species, such as precursors, reaction by-products, and other gases in the processing environment. The process monitoring system 438 components in FIG. 4 are attached to the process chamber 402. In an alternate embodiment, some components of the process monitoring system 438 are located downstream from the process chamber 402. The process monitoring system 438 can be used with controller 436 to determine

the status of the deposition process and provide feedback to ensure process compliance.

[Para 39] The substrate 406 is exposed to the process gas for a time period that results in the desired deposition of the high-k layer. Process conditions that enable the desired deposition of the high-k layer may be determined by direct experimentation and/or design of experiments. For example, adjustable process parameters can comprise time, temperature (e.g., substrate temperature), process pressure, process gases and relative gas flows of the process gases, among other parameters. The process parameter space for the deposition process can, for example, utilize a chamber pressure less than about 10 Torr, a process gas flow rate less than 2000 sccm, a precursor gas flow rate less than 1000 sccm, and a substrate temperature greater than about 200° C.

[Para 40] When depositing a metal oxide high-k dielectric layer using TCVD, a process gas comprising a metal-containing precursor is introduced into a processing chamber containing a heated substrate to be processed. The substrate is exposed to the process gas for a time period that results in the desired deposition of the metal oxide high-k layer. Metal oxide high-k materials can be deposited from metal oxide chemical vapor deposition (MOCVD) precursors. In the exemplary case of Hf and Zr (M=Hf, Zr), the MOCVD precursors can comprise metal alkoxides (e.g., $M(OR)_n$) and metal alkylamides (e.g., $M(NR)_4$) that can deposit metal oxide layers at substrate temperatures above about 300°C. The metal alkoxide precursors can, for example, be selected from four-coordinate complexes such as $M(OMe)_4$, $M(OEt)_4$, $M(OPr)_4$, and $M(OBu^t)_4$, where Me is methyl, Et is ethyl, Pr is propyl, and Bu^t is tert-butyl. The metal alkylamide precursor can, for example, be selected from $M(NMe_2)_4$, $M(NEt_2)_4$, and $M(NPr_2)_4$. The MOCVD precursor can also be selected from six-coordinate complexes such as $M(OBu^t)_2(MMP)_2$ and $M(MMP)_4$, where MMP = $OCMe_2CH_2OMe$. As would be appreciated by those skilled in the art, other metal-containing precursors may be employed without departing from the scope of the invention.

[Para 41] $Hf(OBu^t)_4$ is a hafnium-containing MOCVD precursor that enables deposition of HfO_2 high-k layers for device fabrication. $Hf(OBu^t)_4$ comprises a relatively high vapor pressure (P_{vap}~1Torr at 65°C), and therefore requires minimal heating of the precursor and precursor delivery lines for delivering the precursor to the process chamber. In addition, $Hf(OBu^t)_4$ does not decompose at temperatures below about 200°C, which significantly reduces precursor decomposition due to interactions with chamber walls and gas phase reactions. The $Hf(OBu^t)_4$ precursor can, for example, be delivered to the process chamber using a liquid injection system comprising a vaporizer that is maintained at a temperature of 50°C, or higher. An inert carrier gas (e.g., He,

N_2) can be mixed with the vaporized precursor to aid in the delivery of the precursor to the process chamber.

[Para 42] $Hf(OBu^t)_4$ contains both the Hf metal and the oxygen required to grow stoichiometric HfO_2 layers under proper process conditions, thereby providing reduced process complexity. Alternatively, the process gas containing the MOCVD precursor can further contain a second oxygen-containing gas as a second source of oxygen.

[Para 43] Similarly, metal silicate high-k materials can be deposited from MOCVD precursors and a silicon-containing gas. For example, a $HfSiO_x$ high-k layer can be deposited on a substrate using $Hf(OBu^t)_4$ precursor and a silicon-containing gas. The silicon-containing gas can, for example, contain silane (SiH_4), disilane (Si_2H_6), dichlorosilane (SiH_2Cl_2), hexachlorodisilane (Si_2Cl_6), bis (tertbutylamino) silane ($SiH_2(NBu^t)_2$), or tetrakis (dimethylamino) silane ($Si(NMe_2)_4$), tetraethylorthosilicate (TEOS, $Si(OEt)_4$)), or a combination of two or more thereof.

[Para 44] The process gas can further comprise a carrier gas (e.g., an inert gas) and an oxidizing gas. The inert gas can include at least one of Ar, He, Ne, Kr, Xe, and N_2. The addition of inert gas can, for example, dilute the process gas or adjust the process gas partial pressure(s). The oxidizing gas can, for example, contain an oxygen-containing gas comprising at least one of O_2, O_3, H_2O, H_2O_2, NO, NO_2, and N_2O. The role of the oxygen-containing gas in the deposition process can be to fill any oxygen vacancies in the metal oxide or metal silicate high-k layer, or to chemically modify the metal oxide precursor. The modification can involve interaction of the oxygen-containing gas with the metal oxide precursor in the gas phase or on the deposition surface.

[Para 45] FIGS. 5-8 schematically show plasma processing systems that may be utilized to plasma process a thick complete high-k layer to form a thin complete high-k layer according to embodiments of the invention. FIG. 5 schematically shows a plasma processing system configured for processing a high-k layer according to an embodiment of the invention. The plasma processing system 1 depicted in FIG. 5 is capable of sustaining a plasma and includes a plasma process chamber 10 configured to facilitate the generation of plasma in processing region 45. The plasma processing system 1 further comprises a substrate holder 20 upon which a substrate 25 to be processed is affixed, a gas injection system 40 for introducing process gases 42 to the plasma process chamber 10, an RF generator 30 and impedance match network 32 for delivering RF power to the substrate holder 20, a vacuum pumping system 50, a plasma monitor system 57, and a controller 55.

[Para 46] The gas injection system 40 allows independent control over the delivery of process gases to the process chamber from ex-situ gas sources. An ionizable gas or mixture of gases is introduced via the gas injection system 40 and the process pressure is adjusted. For example, controller 55 is used to control the vacuum pumping system 50 and gas injection system 40.

[Para 47] Substrate 25 is transferred into and out of chamber 10 through a slot valve (not shown) and chamber feed-through (not shown) via a robotic substrate transfer system where it is received by substrate lift pins (not shown) housed within substrate holder 20 and mechanically translated by devices housed therein. Once the substrate 25 is received from the substrate transfer system, it is lowered to an upper surface of the substrate holder 20.

[Para 48] In an alternate embodiment, the substrate 25 is affixed to the substrate holder 20 via an electrostatic clamp (not shown). Furthermore, the substrate holder 20 further includes a cooling system (not shown) including a re-circulating coolant flow that receives heat from the substrate holder 20 and transfers heat to a heat exchanger system (not shown), or when heating, transfers heat from the heat exchanger system. Moreover, gas may be delivered to the backside of the substrate 25 to improve the gas-gap thermal conductance between the substrate 25 and the substrate holder 20. Such a system is utilized when temperature control of the substrate is required at elevated or reduced temperatures. For example, temperature control of the substrate may be useful at temperatures in excess of the steady-state temperature achieved due to a balance of the heat flux delivered to the substrate 25 from the plasma and the heat flux removed from substrate 25 by conduction to the substrate holder 20. In other embodiments, heating elements, such as resistive heating elements, or thermo-electric heaters/coolers are included.

[Para 49] In the embodiment, shown in FIG. 5, the substrate holder 20 can further serve as an electrode through which radio frequency (RF) power is coupled to plasma in the processing region 45. For example, the substrate holder 20 can be electrically biased at a RF voltage via the transmission of RF power from an RF generator 30 through an impedance match network 32 to the substrate holder 20. The RF bias serves to heat electrons and, thereby, form and maintain plasma. In this configuration, the system operates as a RIE reactor, wherein the chamber and upper gas injection electrode serve as ground surfaces. A typical frequency for the RF bias ranges from 1 MHz to 100 MHz and is preferably 13.56 MHz.

[Para 50] In an alternate embodiment, RF power can be applied to the substrate holder electrode at multiple frequencies. Furthermore, the impedance match network 32 serves to maximize the transfer of RF power to plasma in processing chamber 10 by minimizing the reflected power. Match network topologies (e.g., L-type, π–type, T-type) and automatic control methods are known in the art.

[Para 51] With continuing reference to FIG. 5, a process gas 42 is introduced to the processing region 45 through the gas injection system 40. Gas injection system 40 can include a showerhead, wherein the process gas 42 is supplied from a gas delivery system (not shown) to the processing region 45 through a gas injection plenum (not shown), a series of baffle plates (not shown) and a multi-orifice showerhead gas injection plate (not shown).

[Para 52] Vacuum pump system 50 can include a turbo-molecular vacuum pump (TMP) capable of a pumping speed up to 5000 liters per second (and greater), and a gate valve for throttling the chamber pressure. In conventional plasma processing devices utilized for dry plasma etch, a 1000 to 3000 liter per second TMP is employed. TMPs are useful for low pressure processing, typically less than 50 mTorr. For high pressure processing (i.e., greater than 100 mTorr), a mechanical booster pump and dry roughing pump are used.

[Para 53] A controller 55 includes a microprocessor, a memory, and a digital I/O port capable of generating control voltages sufficient to communicate and activate inputs to the plasma processing system 1 as well as monitor outputs from the plasma processing system 1. Moreover, the controller 55 is coupled to and exchanges information with the RF generator 30, the impedance match network 32, the gas injection system 40, plasma monitor system 57, and the vacuum pump system 50. A program stored in the memory is utilized to control the aforementioned components of a plasma processing system 1 according to a stored process recipe. One example of controller 55 is a digital signal processor (DSP); model number TMS320, available from Texas Instruments, Dallas, Texas.

[Para 54] The plasma monitor system 57 can comprise, for example, an optical emission spectroscopy (OES) system to measure excited particles in the plasma environment and/or a plasma diagnostic system, such as a Langmuir probe, for measuring plasma density. The plasma monitor system 57 can be used with controller 55 to determine the status of the etching process and provide feedback to ensure process compliance. Alternately, plasma monitor system 57 can comprise a microwave and/or a RF diagnostic system.

[Para 55] FIG. 6 schematically shows a plasma processing system configured for processing a high-k layer according to another embodiment of the invention. The plasma processing system 2 of FIG. 6 includes the components of system 1 depicted in and described with reference to FIG. 5, and further includes either a mechanically or electrically rotating DC magnetic field system 60 to potentially increase plasma density and/or improve plasma processing uniformity. Moreover, the controller 55 is coupled to the rotating magnetic field system 60 in order to regulate the speed of rotation and the field strength.

[Para 56] FIG. 7 schematically shows a plasma processing system configured for processing a high-k layer according to yet another embodiment of the invention. The plasma processing system 3 of FIG. 7 includes the components of system 1 depicted in and described with reference to FIG. 5, and further includes an upper plate electrode 70 to which RF power is coupled from an RF generator 72 through an impedance match network 74. A typical frequency for the application of RF power to the upper electrode ranges from 10 MHz to 200 MHz, for example 60 MHz. Additionally, a typical frequency for the application of power to the substrate holder 20 ranges from 0.1 MHz to 30 MHz, for example 2 MHz. Moreover, the controller 55 is coupled to the RF generator 72 and the impedance match network 74 in order to control the application of RF power to the upper electrode 70.

[Para 57] FIG. 8 schematically shows a plasma processing system configured for processing a high-k layer according to still another embodiment of the invention. The plasma processing system 4 of FIG. 8 includes the components of system 1 depicted in and described with reference to FIG. 5, and further includes an inductive coil 80 to which RF power is coupled via an RF generator 82 through an impedance match network 84. RF power is inductively coupled from the inductive coil 80 through a dielectric window (not shown) to the plasma-processing region 45. A typical frequency for the application of RF power to the inductive coil 80 ranges from 10 MHz to 100 MHz, for example 13.56 MHz. Similarly, a typical frequency for the application of power to the substrate holder 20 ranges from 0.1 MHz to 30 MHz, for example 13.56 MHz. In addition, a slotted Faraday shield (not shown) can be employed to reduce capacitive coupling between the inductive coil 80 and plasma. Moreover, the controller 55 is coupled to the RF generator 82 and the impedance match network 84 in order to control the application of power to the inductive coil 80.

[Para 58] In an alternate embodiment, the plasma is formed using electron cyclotron resonance (ECR). In yet another embodiment, the plasma is formed from the

launching of a Helicon wave. In yet another embodiment, the plasma is formed from a propagating surface wave.

[Para 59] Numerous modifications and variations of the invention are possible in light of the above teachings. It is therefore to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.